Signal Integrity and EMC Considerations In PCB Design

Introduction

This course stresses hands-on techniques for the design and layout of printed circuit boards. Signal Integrity and Electromagnetic Compatibility (EMC) along with regulatory compliance requirements will be examined. Signal integrity is a primary concern for system functionality, while EMC compliance allows a product to be legally sold. This course was developed for both experienced and junior level engineers who are responsible for printed circuit board designs and system level products.

The participant, upon completion, should be able to create a high-density, high technology printed circuit board that meets or exceeds test and system level requirements without rework. Design and layout techniques of several years ago are now insufficient to address today's high speed, high technology products for both signal integrity and EMC.

In an informal atmosphere, design and layout techniques are introduced in an easy to follow step-by-step presentation that allows plenty of opportunities to address specific questions. Major instructional emphasis is placed on real-life examples that demonstrate good layout practices that can be incorporated immediately into your designs.

Course Objective

This course presents both simplified theory and "rules-driven, hands-on techniques" for enhancement of signal integrity along with suppression of RF energy (EMI) created within the printed circuit board. The focus is at the *fundamental* level. Rigorous mathematical analysis and theory will *not* be presented. The course is geared toward multi-layer, high-density designs. Requirements for single- and double-sided designs are examined based upon fundamental concepts for multi-layer boards.

The objective is to allow engineers to understand how a PCB functions as a transmission line between devices, how RF energy is created, and to provide insight into concepts and tools that assist in optimizing a design during the layout and debug cycle. Proper layout not only assures functionality, but also allows for compliance with EMC requirements plus compatibility between electrical systems within a product to ensure operation for the life of the unit, both commercial and military applications.

The discussion on EMC, which is a major part of this course, is based on implementing RF suppression at the circuit level instead of relying on system level containment for emissions and immunity.

Who Should Attend

This course is intended for *practicing* design engineers of all disciplines, regulatory compliance engineers, EMC consultants and PCB designers. No formal training in electronic theory is required. Concepts, theory and layout techniques are presented in an easy to understand format, *without math*, using practical and real world examples. Engineers, technicians, supervisors and managers can also gain valuable insights into PCB design and layout for today's high technology products along with obstacles that exist for the designer.

Benefits of Attending

- Increased Job Knowledge
- Enhanced Signal Integrity
- Teaches EMC Suppression versus Containment
- Allows First-Time Compliance to EMC Requirements
- Reduce Design Time and Manufacturing Costs
- State-of-the-Art Design and Layout Techniques Presented

Signal Integrity & EMC Considerations in PCB Design

(One Day Seminar)

Fundamentals of Signal Integrity

- Transmission Line Equivalent Circuit
- Relative Permittivity (Dielectric Constant)
- Propagation Delay Within Various Materials
- Chart of FR-4 Material
- Ringing and Reflections
- Typical Transmission Line System
- Identification of Signal Distortion
- Crosstalk
- Design Techniques to Prevent Crosstalk
- Power and/or Ground Bounce
- Typical Bounce Waveform
- Component Selection Related to EMC

Fundamentals of EMC

- Component Characteristics at RF Frequencies
- How Printed Circuit Boards Create EMI
- Right Hand Rule
- Maxwell's Equations
- Closed Loop Circuit
- Radiated Emissions from a Closed Loop Circuit
- Loop Area Between Components
- Common-Mode and Differential-Mode Currents
- Basic Concept for EMC Suppression
- Summary of EMI Development Within PCBs

Bypassing and Decoupling

- Defining Capacitor Usage
- Purpose of Using Capacitive Structures
- Capacitors and Resonance
- Using Capacitors in Parallel
- Effects of Capacitors in Parallel
- Power and Ground Plane Capacitance
- Capacitive Loops Created by Decoupling Capacitors
- Placement Recommendations

Layer Stackup Assignment

- Single and Double-Sided Recommended Layout
- Multi-Layer Stackup Assignments
- Film and Manufacturing Concerns

Impedance Control and Trace Routing

- Impedance Control Equations
- Capacitive Loading
- Calculating Maximum Trace Length for Trace Routing
- Routing Layers
- Layer Jumping - Use of Vias
- Trace Separation and *the 3-W Rule*
- Guard and Shunt Traces

Terminations (Signal Integrity Concerns)

- Fundamental Concepts of Trace Termination
- Transmission Line Effects
- Termination Methodologies
- Where to Locate Terminators
- What Happens When One Cannot Terminate
- Fundamental Reasons Why EMI is Developed

Crossing the Barrier

- Isolation (Moating), Bridging and Violations

Electrostatic Discharge (ESD Protection)

- Description of an ESD Event
- ESD Waveforms and Triboelectric Series
- Comparision of Various Voltage Levels
- Failure Modes for ESD
- Design Technique for ESD Protection
- Circuit Layout Techniques
- System Level Protection
- Guard Bands